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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,611	02/12/2004	Hiroshi Fujita	118630	3942

25944 7590 09/09/2005

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EXAMINER	
GRANT, ROBERT J	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,611	FUJITA ET AL.	
	Examiner	Art Unit	
	Robert Grant	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 page 2-12-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimamoto et al. (US 6,362,627) in view Kadouchi et al. (Us 6,020,717).

As to Claim 1, Shimamoto dicloses a voltage detecting apparatus for a combination battery comprising: a multiplexer type flying capacitor voltage detecting circuit having an input multiplexer and an output side sampling switch (Figure 4), whose operation timing is controlled in response to an entered switching control signal for time sequentially executing voltage read-in processing and voltage read-out processing to detect the voltage of a plurality of battery modules of a combination battery in a time sequential fashion (Column 9, lines 26-30); a synchronous control type A/D converter whose operation timing is controlled in response to an entered activation signal for sample holding and A/D converting an analog output voltage of said flying capacitor voltage detecting circuit, and holding a digital voltage signal as a resulting output until a succeeding digital voltage signal is obtained (Column 4, lines 4-13); and a battery controller whose operation timing is controlled in response to an entered transfer command signal for reading said digital voltage signal produced from said A/D converter

(Column 8, lines 51-56), wherein said battery controller comprises a timing table on which generation timings of said switching control signal, said activation signal, and said transfer command signal are all determined on a common time axis (Figure 5), and timing control for said flying capacitor voltage detecting circuit, said A/D converter, and said battery controller is carried out by outputting said switching control signal, said activation signal, and said transfer command signal to said flying capacitor voltage detecting circuit, said A/D converter, and said battery controller at the timing regulated in said timing table and according to an order memorized in said timing table (figure 5). Shimamoto does not expressly disclose storing the readout digital voltage signal into a data storage area assigned to each of said battery modules. Kadouchi discloses and storing the readout digital voltage signal into a data storage area assigned to each of said battery modules (Column 5, lines 24-25). It would have been obvious to a person having ordinary skill in the art at the time of this invention to use Kadouchi's digital system to digitally store the voltage values so that they are easily accessible to computer systems for reading and analysis.

Allowable Subject Matter

3. Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claim 5 is allowed.

Claim 2 recites, inter alia, the battery controller gives priority to the signal applied to the flying capacitor voltage detecting circuit when the time of the switching control signal equals or overlaps the generation timing of the activation signal or the transfer command signal.

Claim 3 recites, inter alia, the timing is configured such that the voltage read-in timing of the A/D converter does not involve the switching timing of the flying capacitor voltage detecting circuit and the data storage.

Claim 4 recites, inter alia, a first timing table for the switching control signal, second table for activation signal and transfer command signal, and the battery control refers to the first time table in time interval shorter than those of said second table.

Claim 5 recites, inter alia, a flying capacitor voltage detecting apparatus using a multiplexer, A/D converter, and battery controller. The controller writes identification numbers of battery modules into a read out memory table in order of the highest to lowest voltage, then battery controller controls the input of the multiplexer of the flying capacitor voltage detecting circuit such that in the next voltage read out processing the voltages are read out according to the order in which they were memorized in the memory table. The art of record does not disclose, teach or suggest the above limitation.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Grant whose telephone number is 571-272-2727. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RG

9/6/05

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
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